

FIG. 1

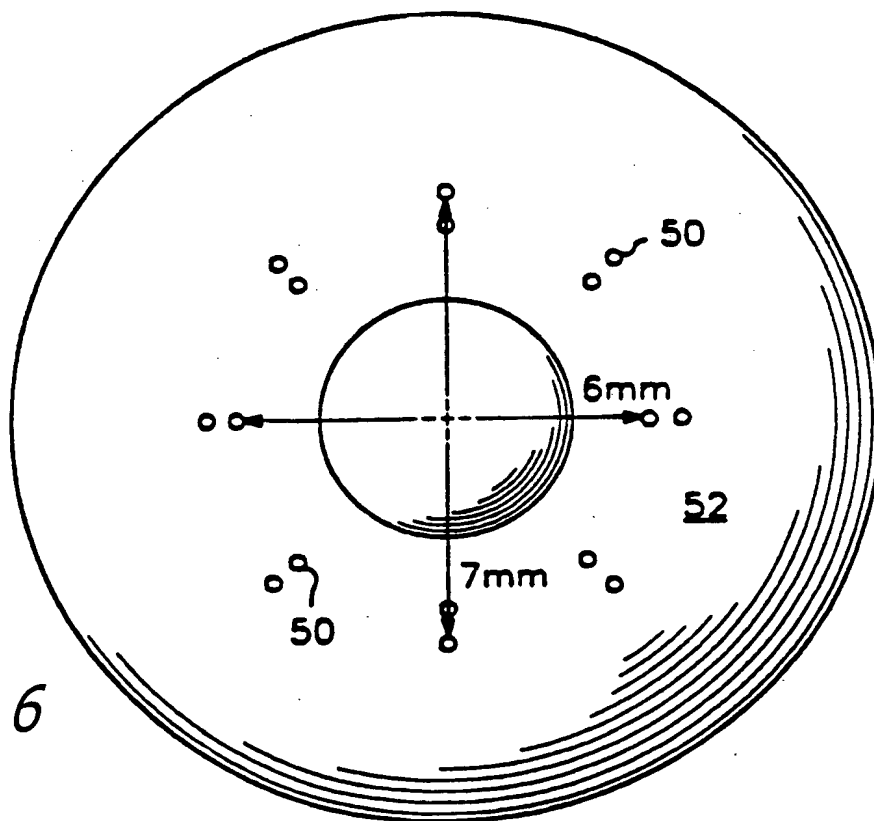


FIG. 6

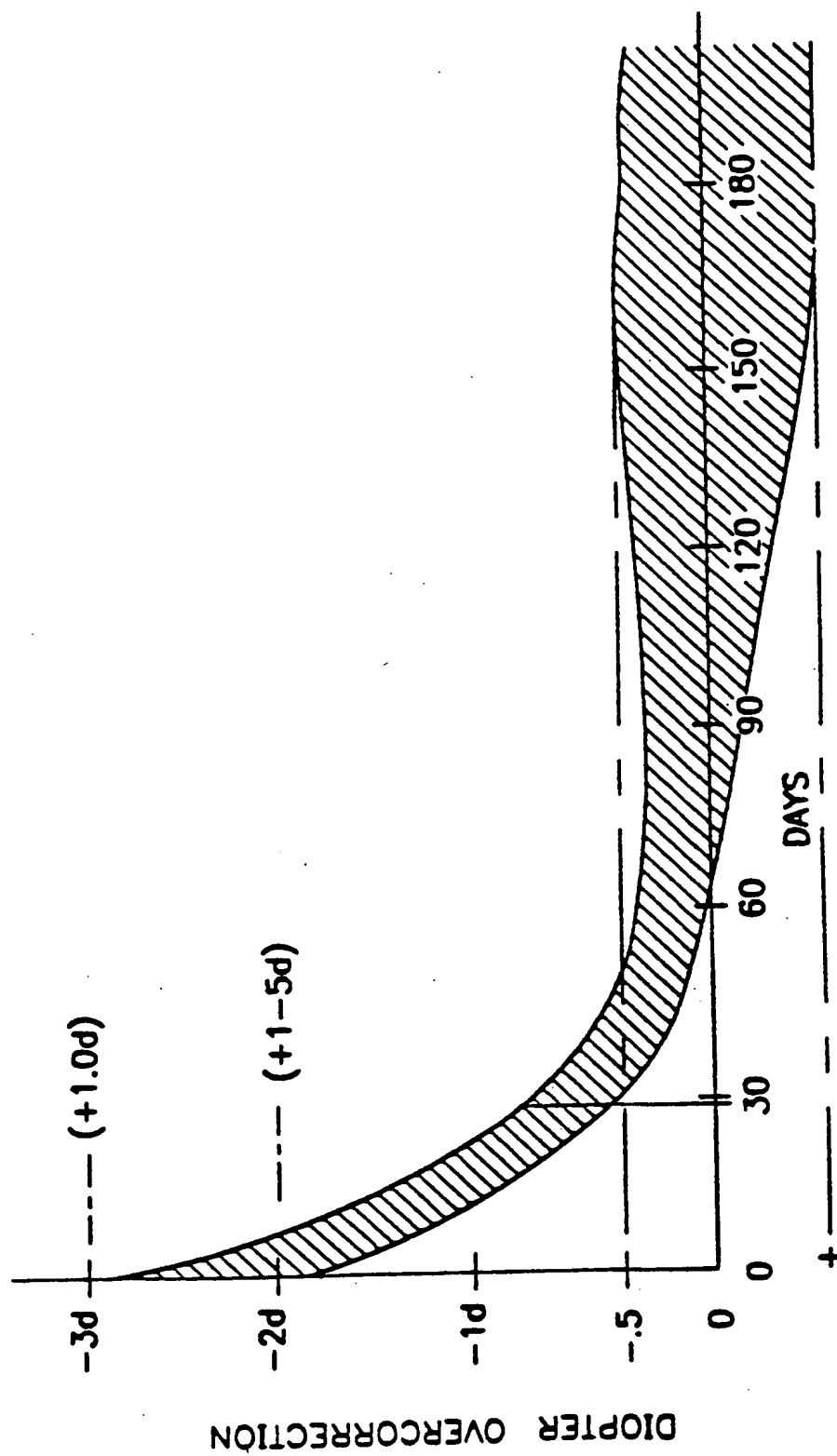


FIG. 1b

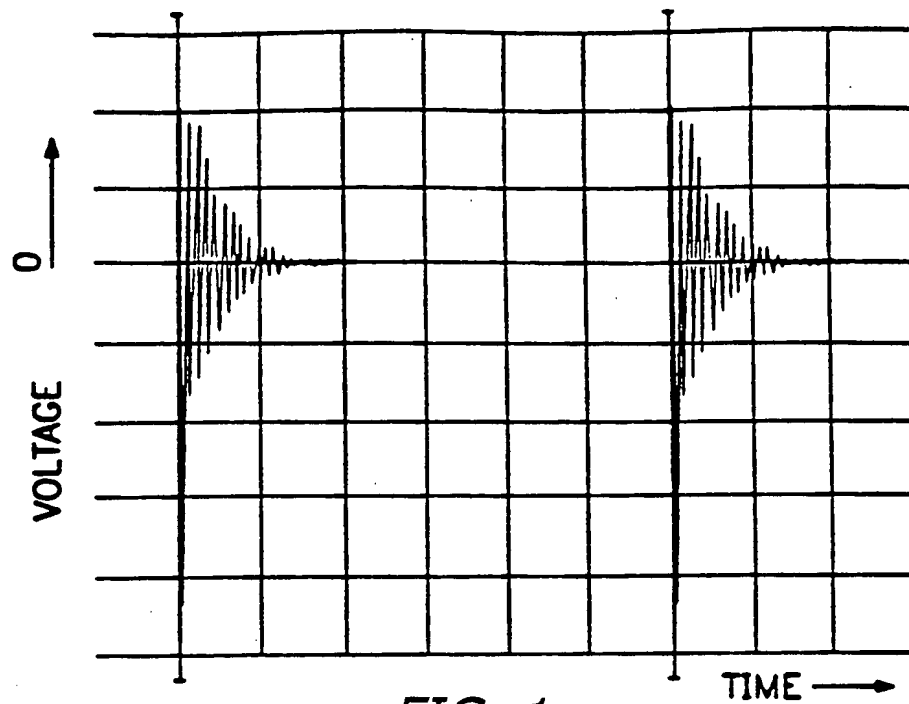


FIG. 1a

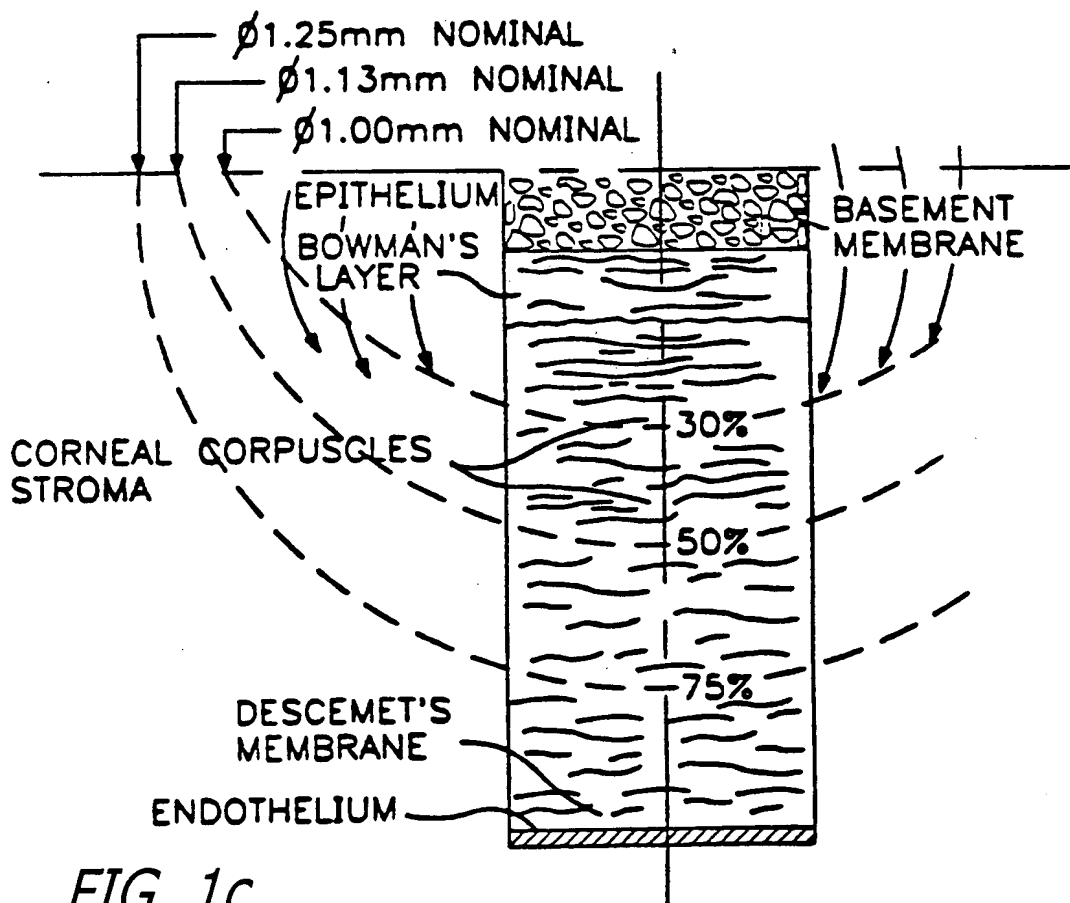
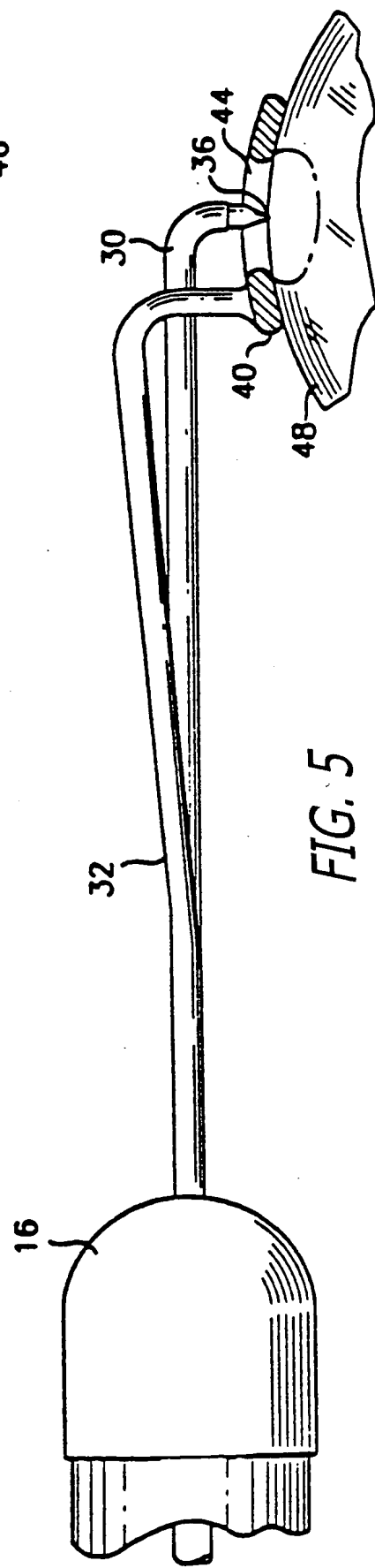
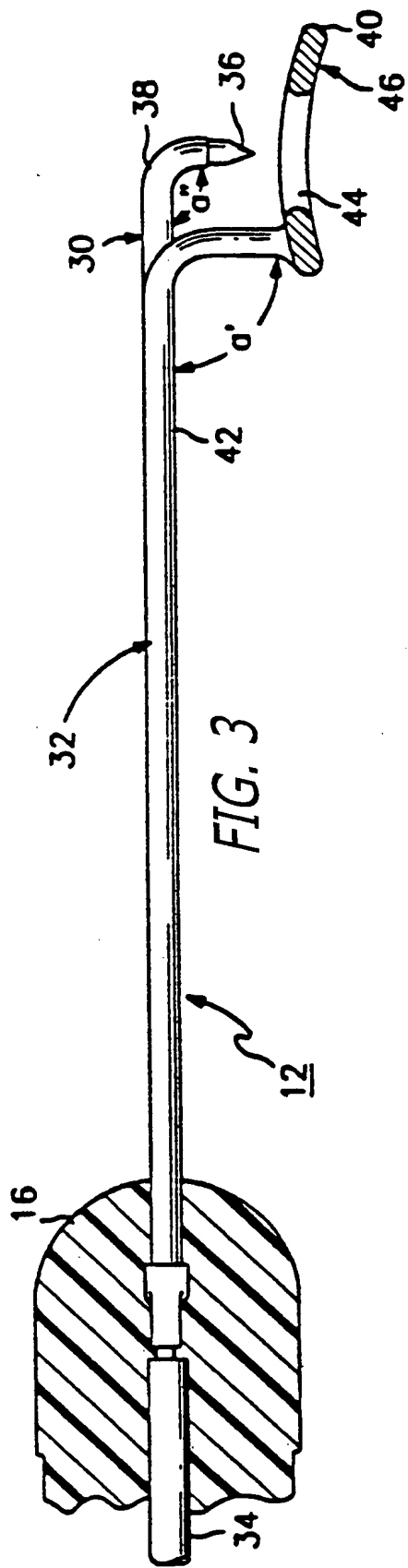
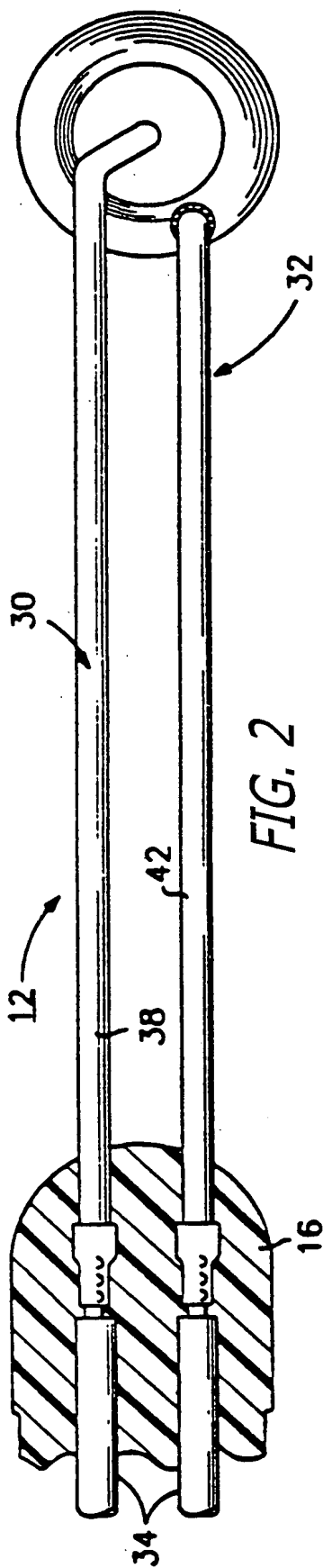


FIG. 1c



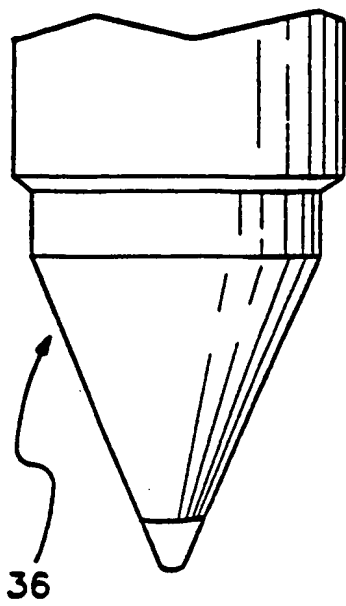


FIG. 4

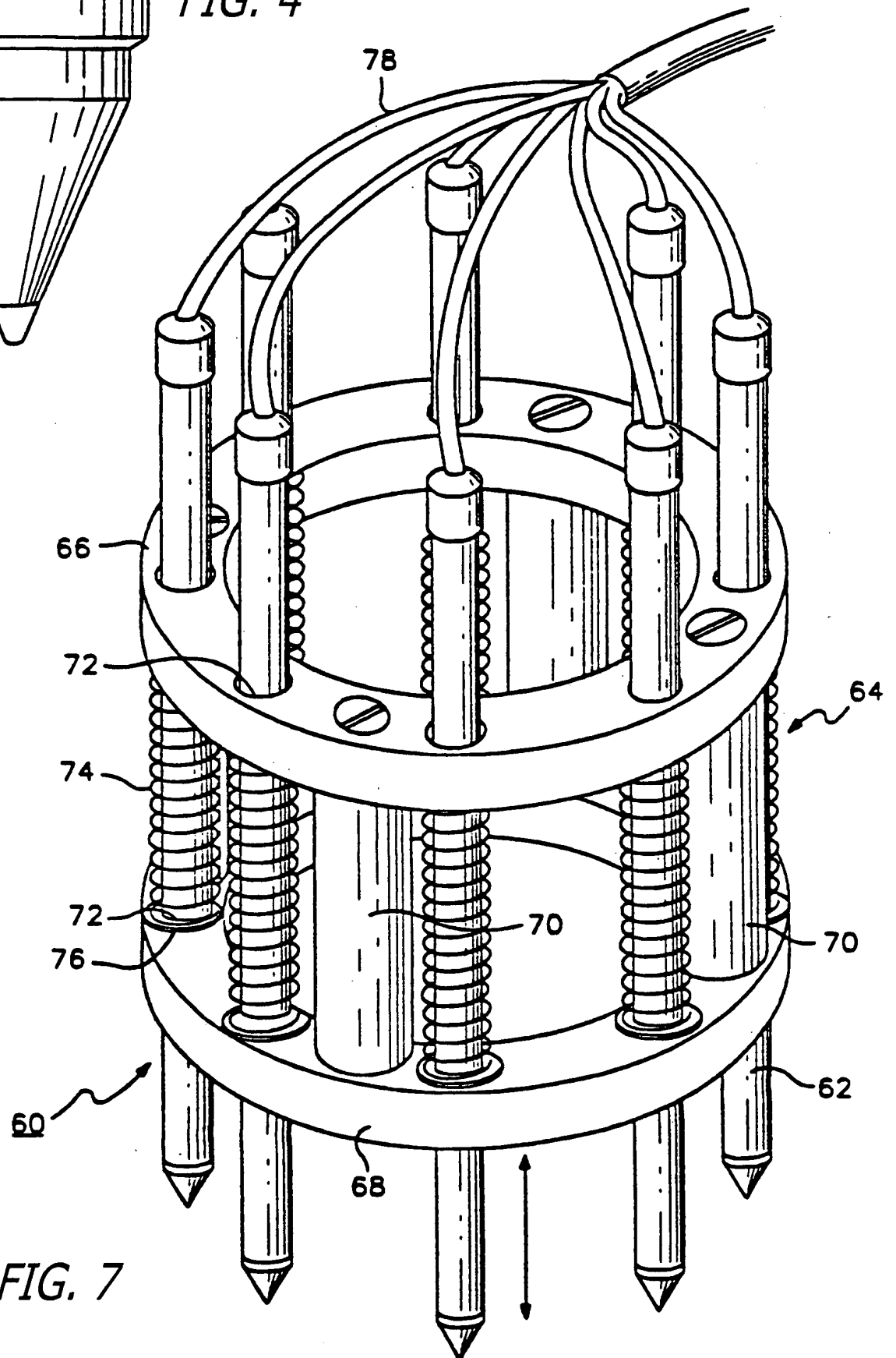


FIG. 7

FIG. 8a

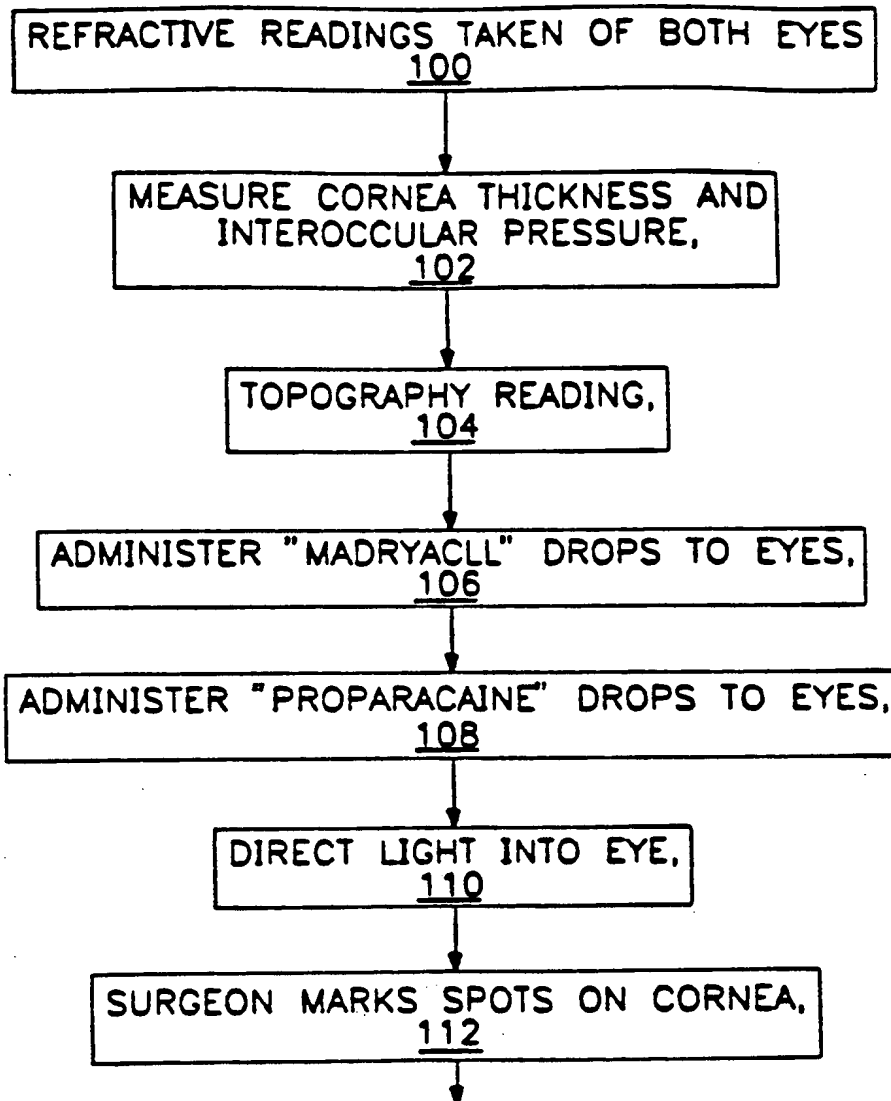
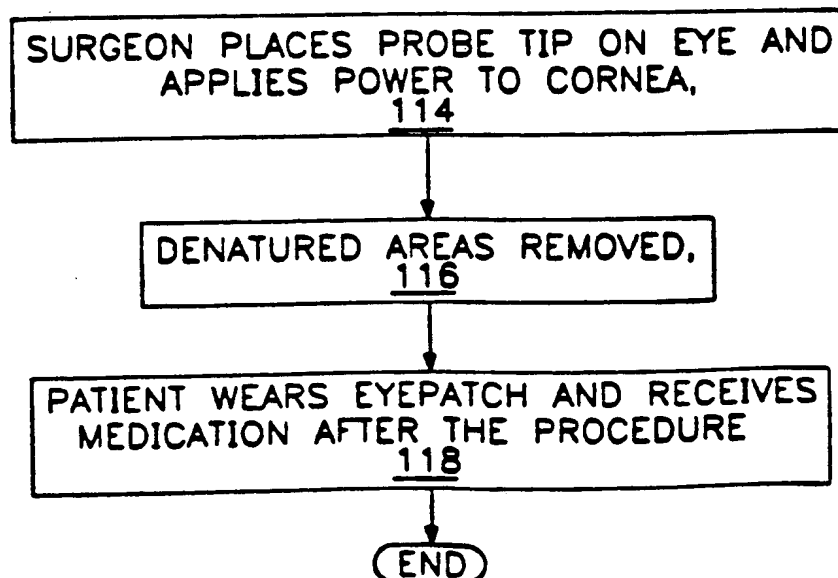


FIG. 8b



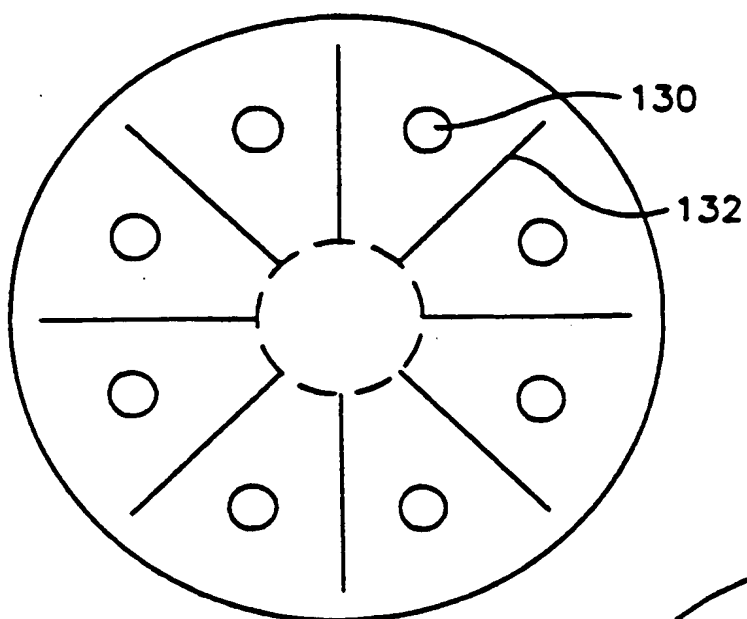


FIG. 9

FIG. 10

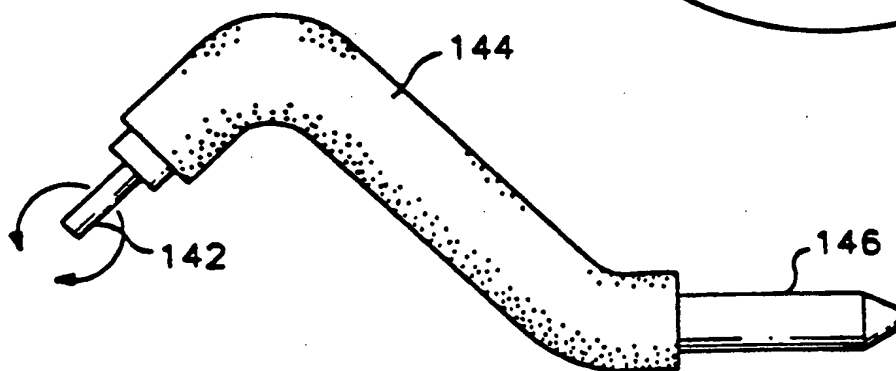
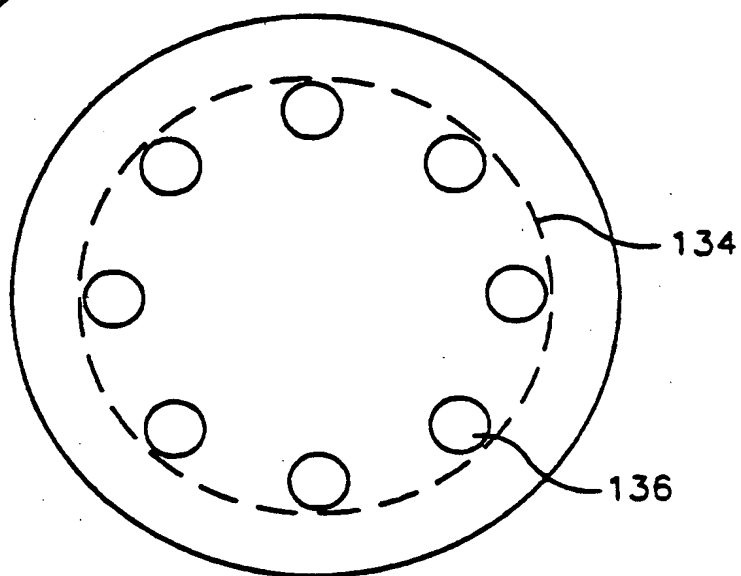


FIG. 11

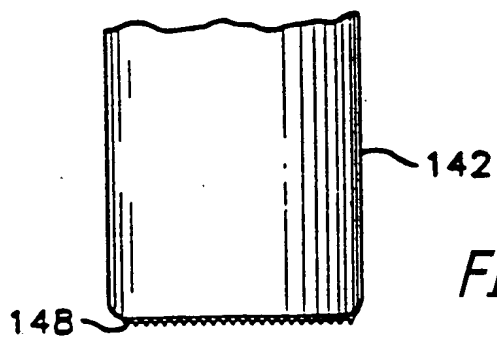
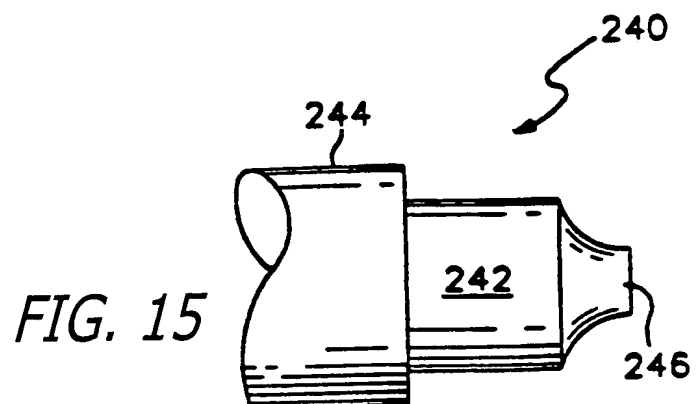
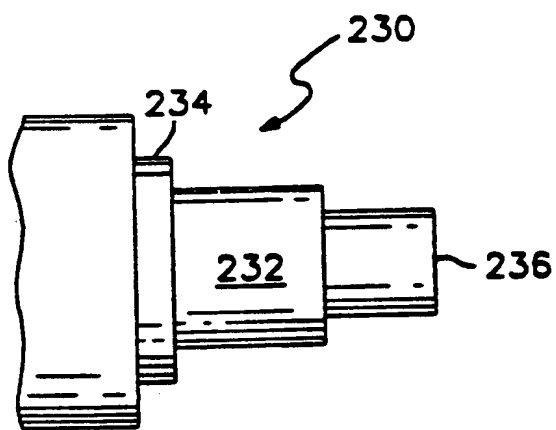
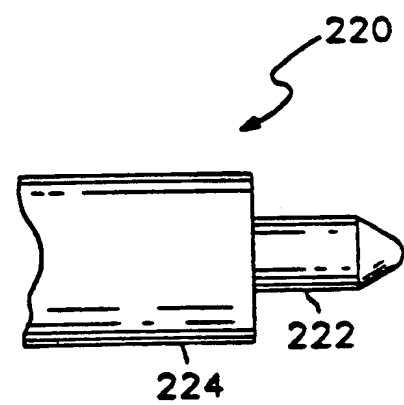
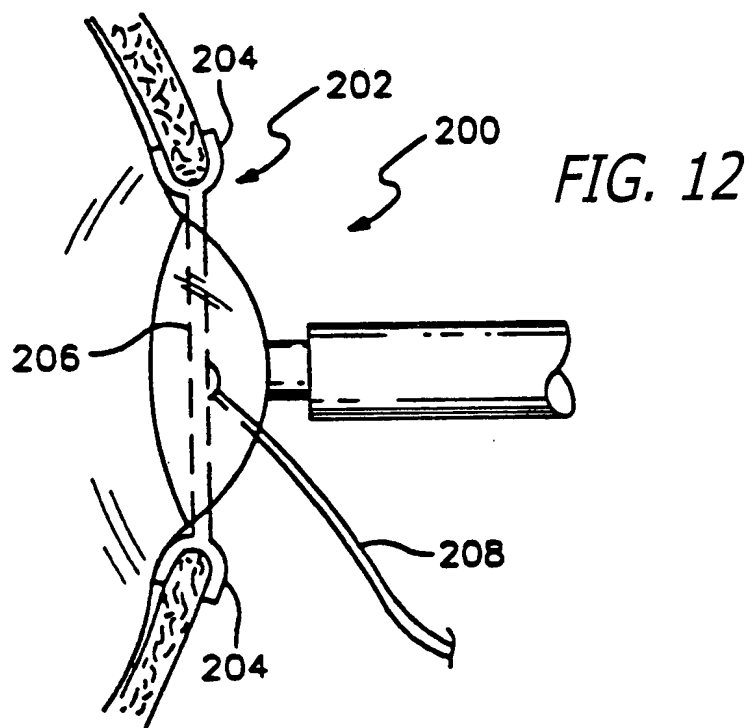


FIG. 11a





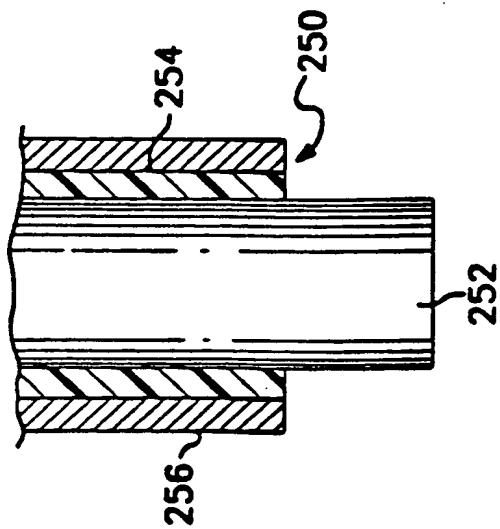


FIG. 16

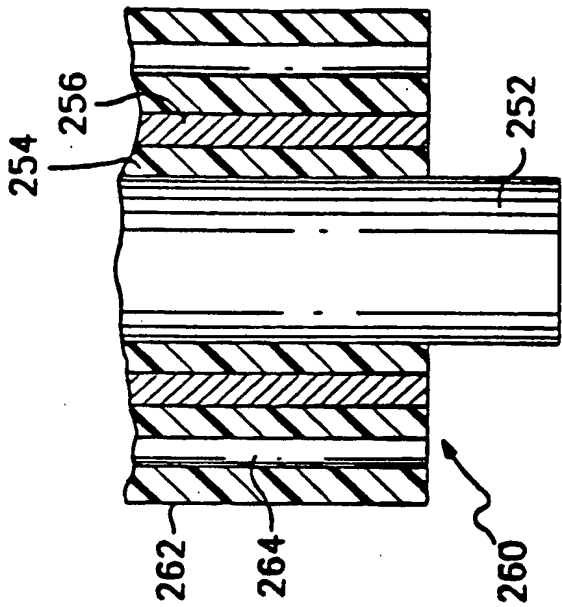


FIG. 17

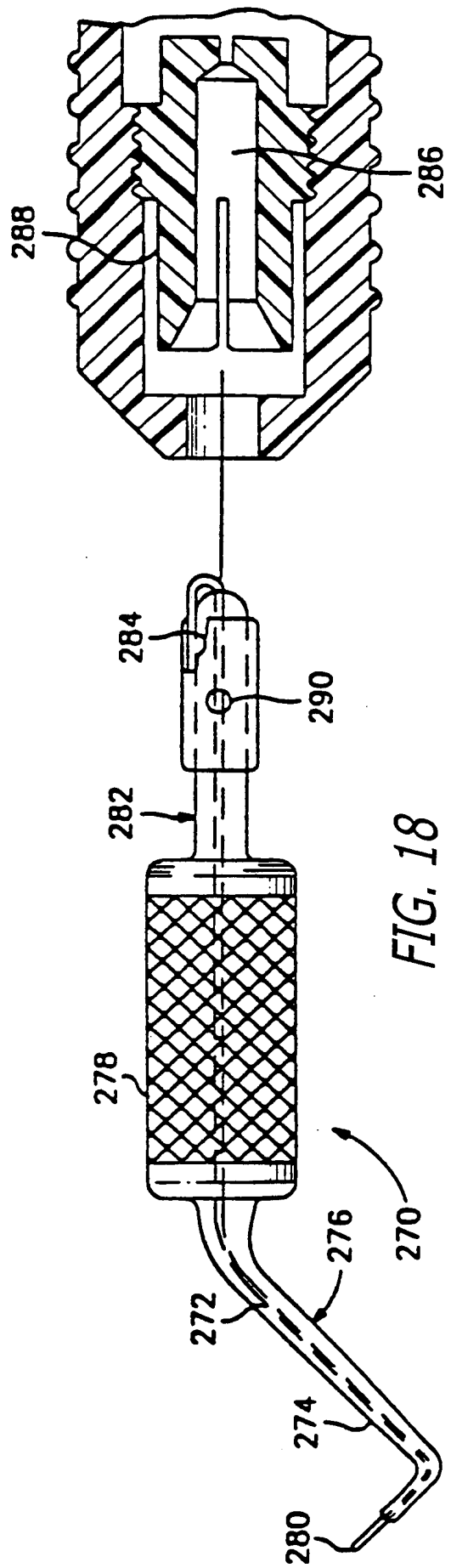


FIG. 18

**FIG. 19**

300

14

22

(I=1/5 302 RATING)

20

V++

V++

Vcc

GND

DATA INPUT

CLOCK INPUT

OUTPUT ENABLE

Vcc

GND

ALL COMPONENTS THIS SIDE ARE INSIDE 14

ALL COMPONENTS THIS SIDE ARE MOUNTED IN CONNECTOR/PLUG 20

FIG. 19 is a schematic diagram of a relay-based digital circuit. The circuit is divided into two sections by a dashed line. The left section, labeled '14', contains a relay assembly 300 with a coil 301, a normally closed contact 312, and a normally open contact 310. The coil is connected to a V++ supply through a resistor R1 (301) and a current I. The normally closed contact 312 is connected to a V++ supply through a resistor R2. The normally open contact 310 is connected to a V++ supply. The right section, labeled '20', contains three D-type flip-flops 306. Each flip-flop has a clock input (CLK), a data input (D), and an output (Q). The outputs of the flip-flops are connected to a Vcc supply. The circuit is powered by a V++ supply and a Vcc supply. A dashed line separates the components inside the connector/plug 20 from those mounted on the side of the connector/plug 20.

**ALL COMPONENTS  
THIS SIDE ARE  
INSIDE 14**

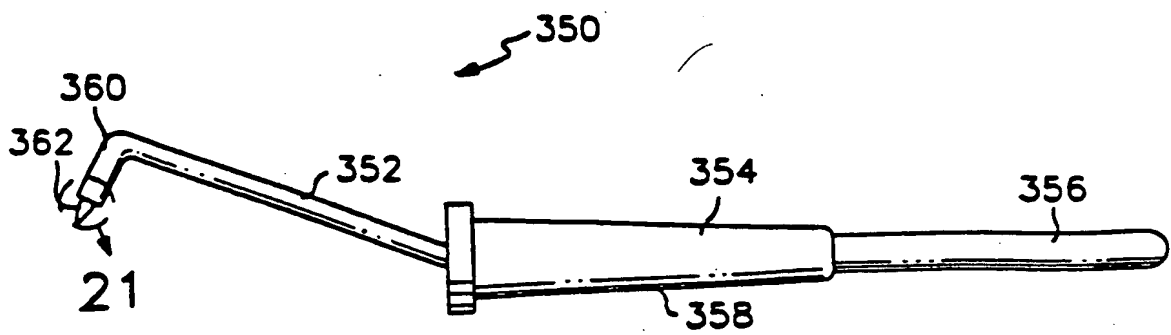


FIG. 20

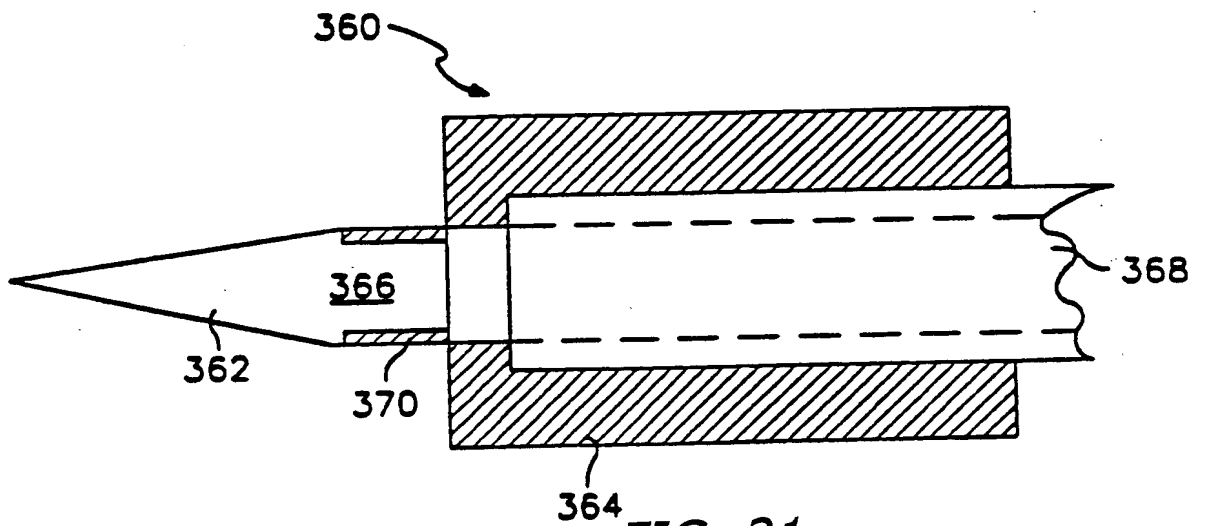


FIG. 21

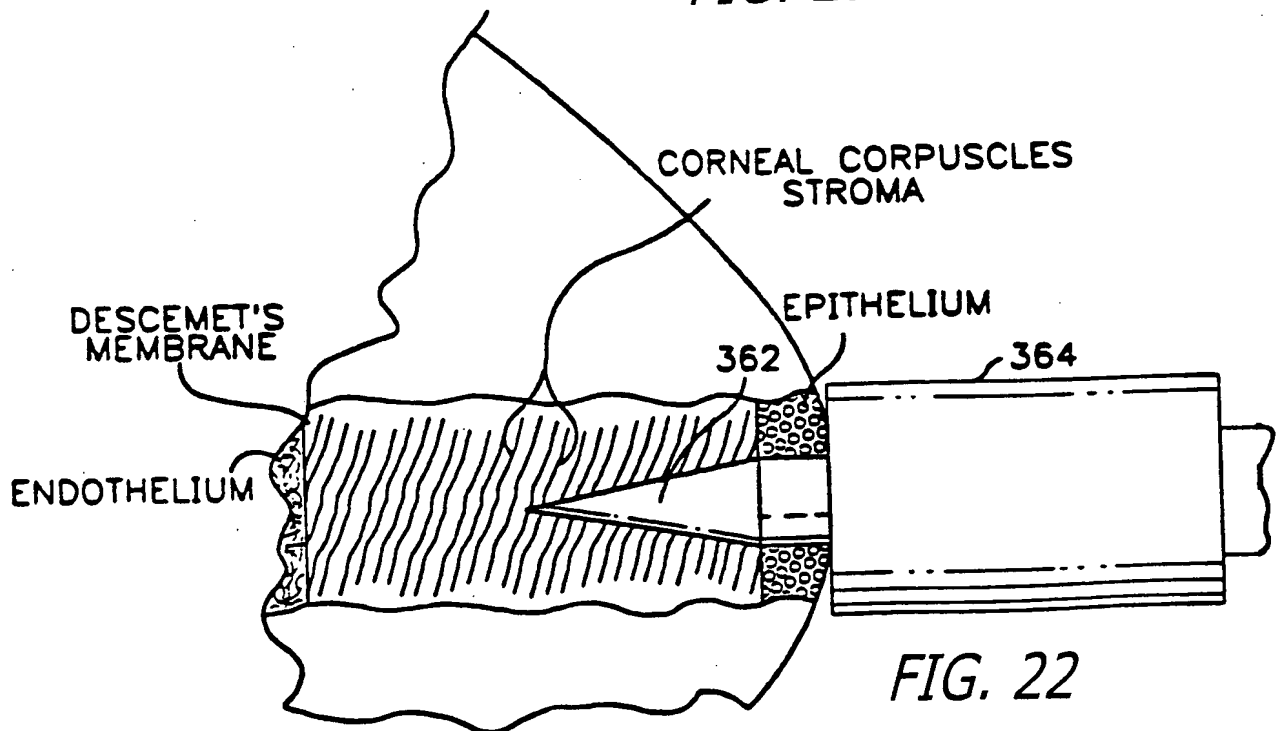
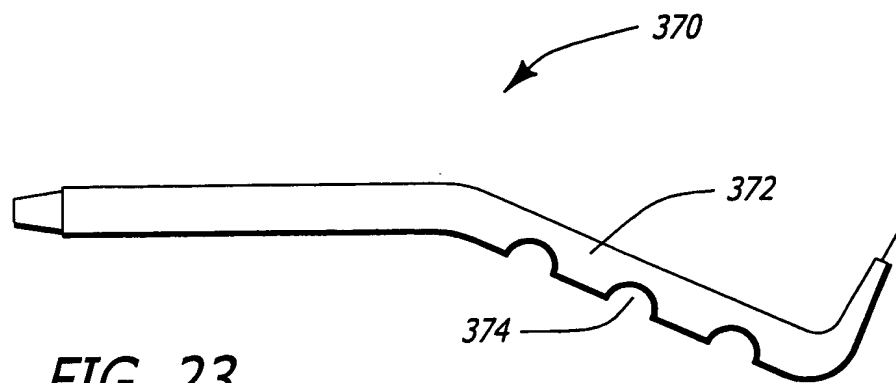
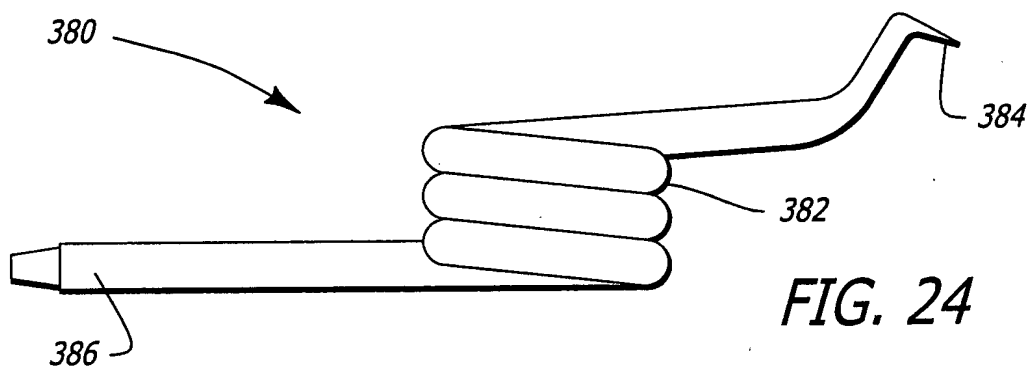


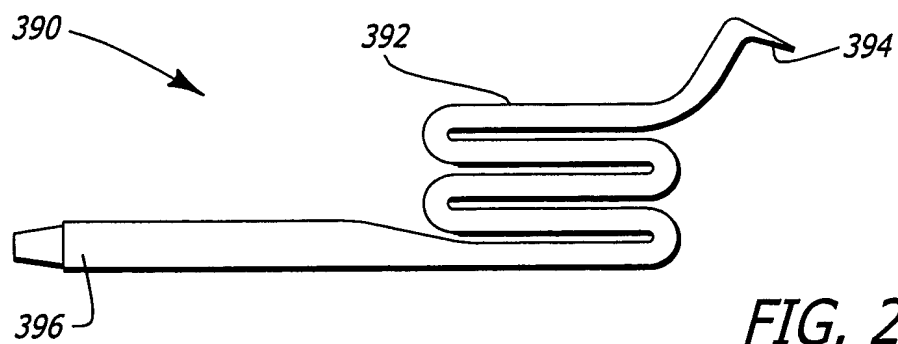
FIG. 22



**FIG. 23**



**FIG. 24**



**FIG. 25**

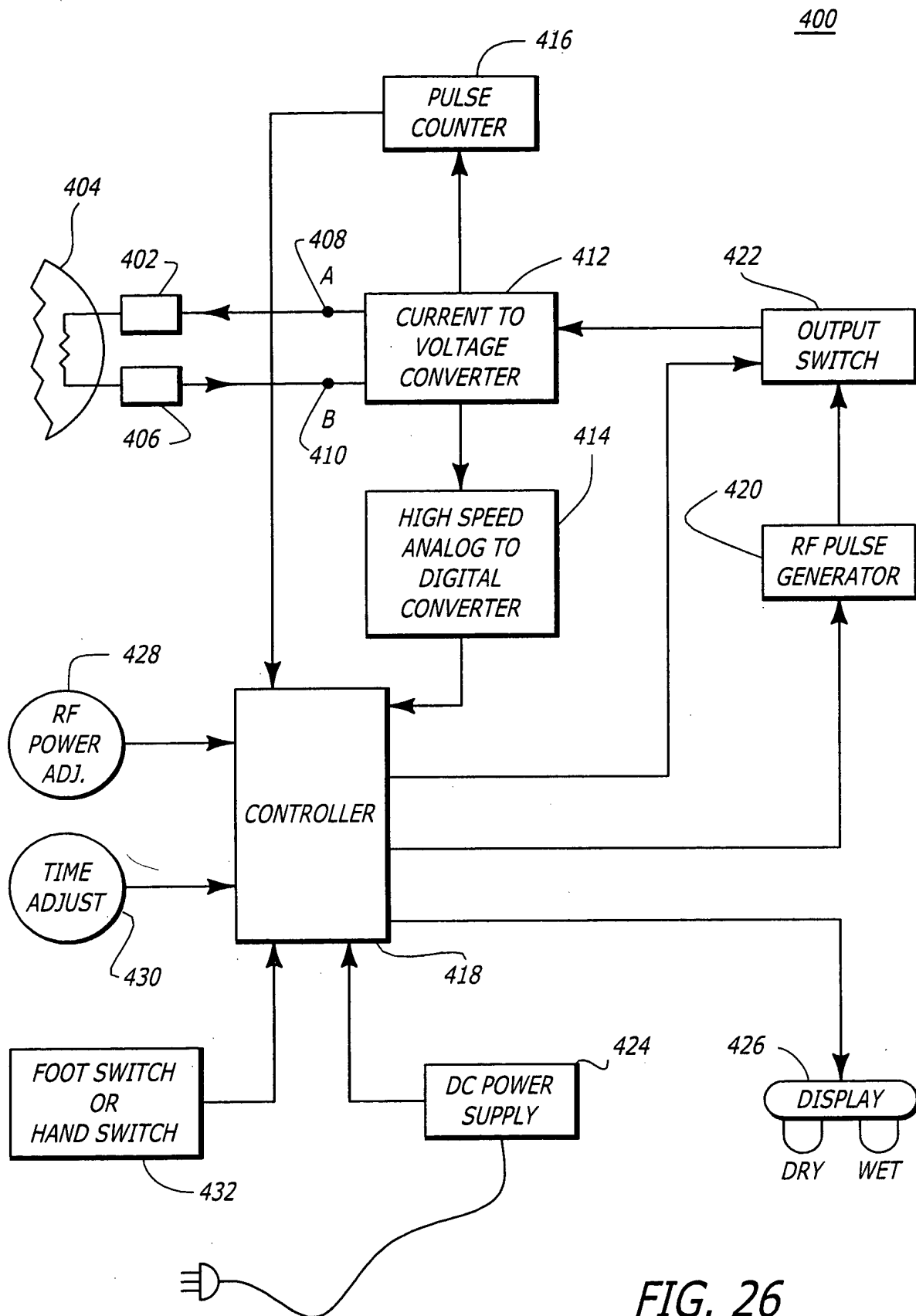
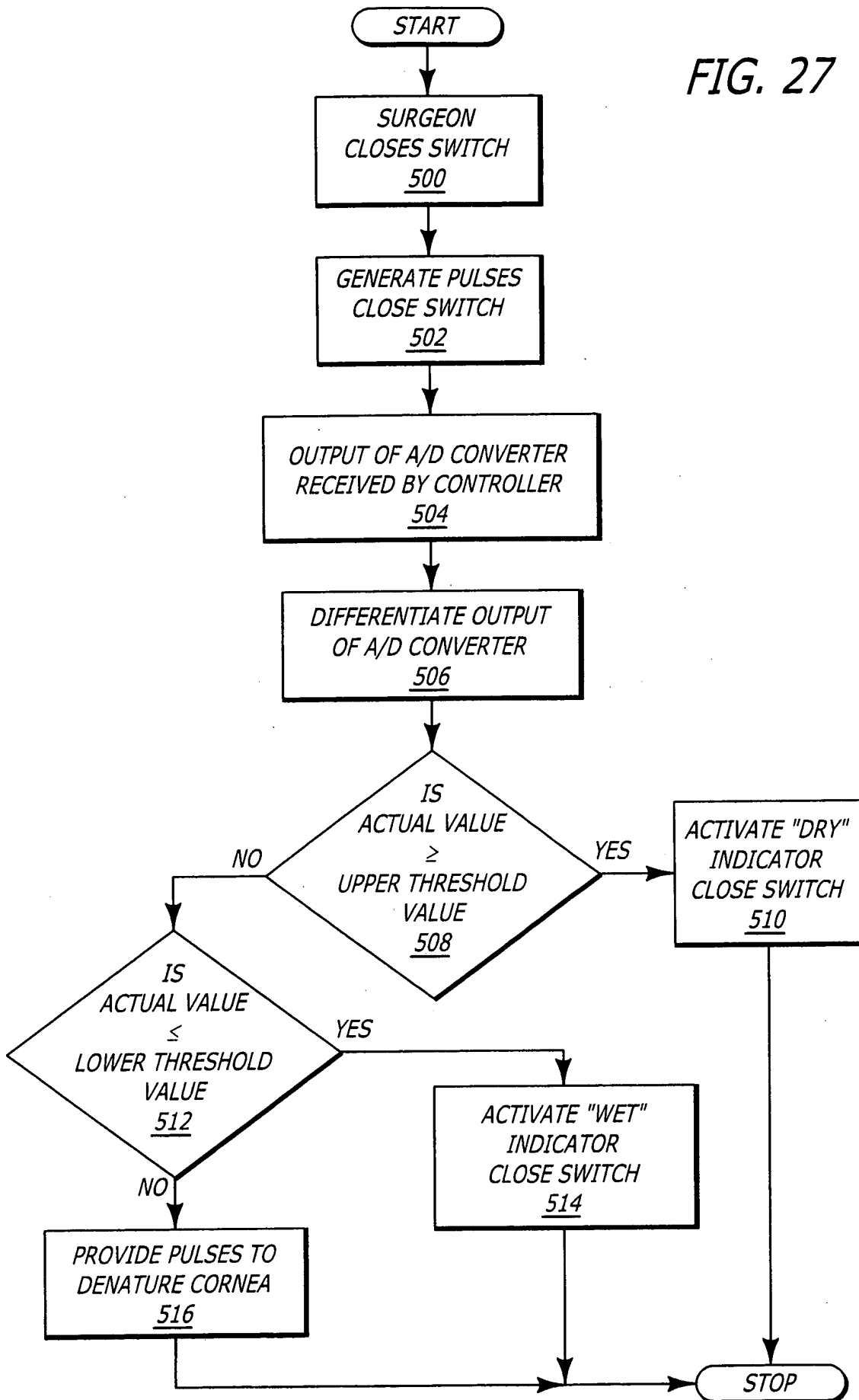
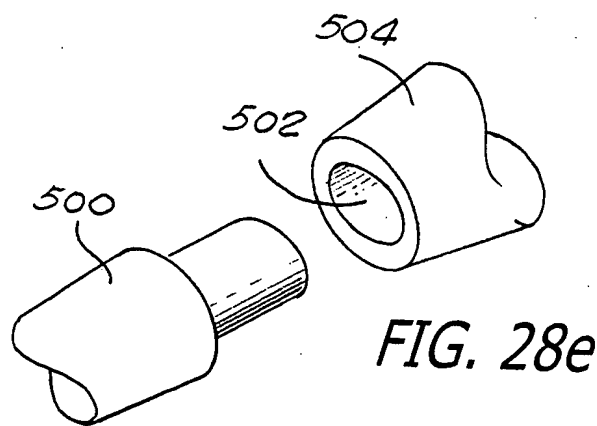
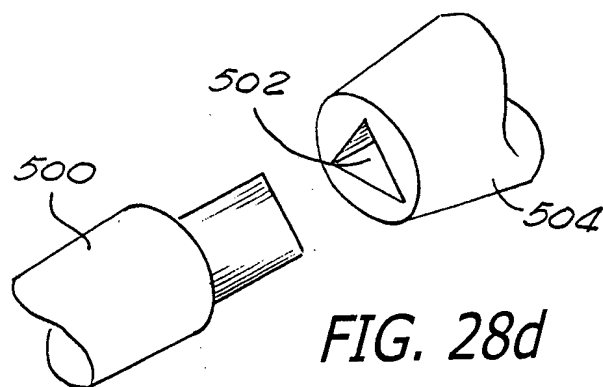
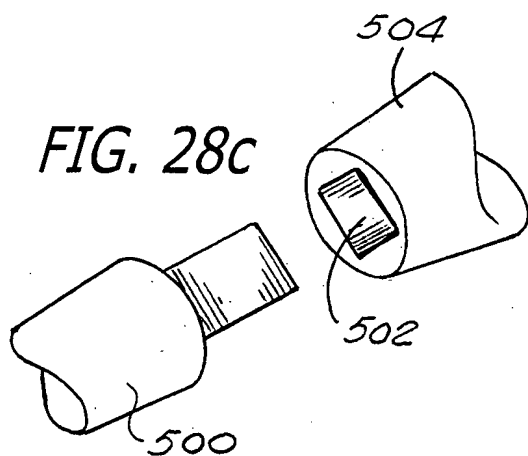
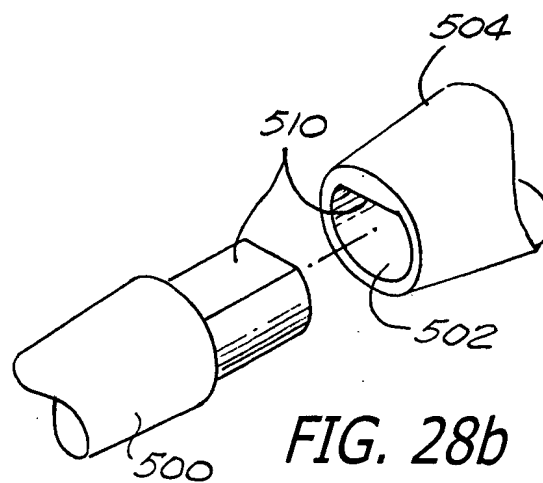
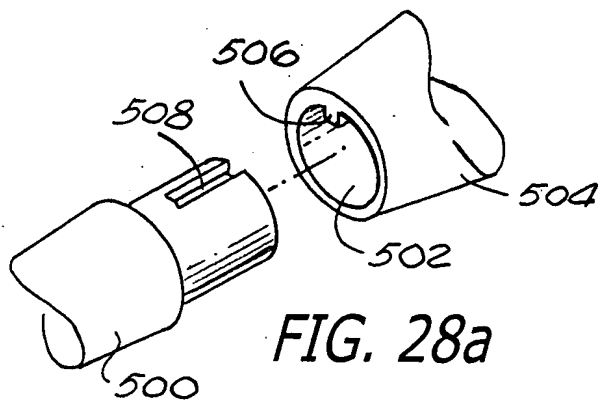
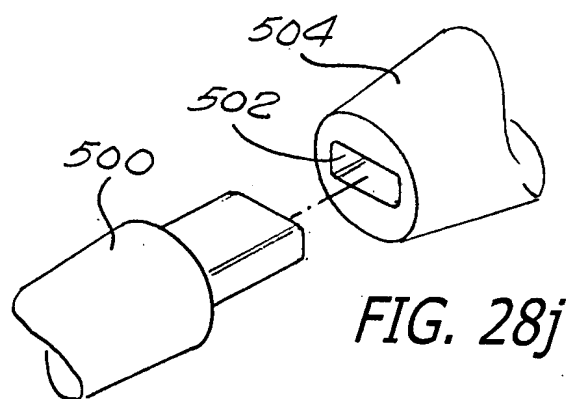
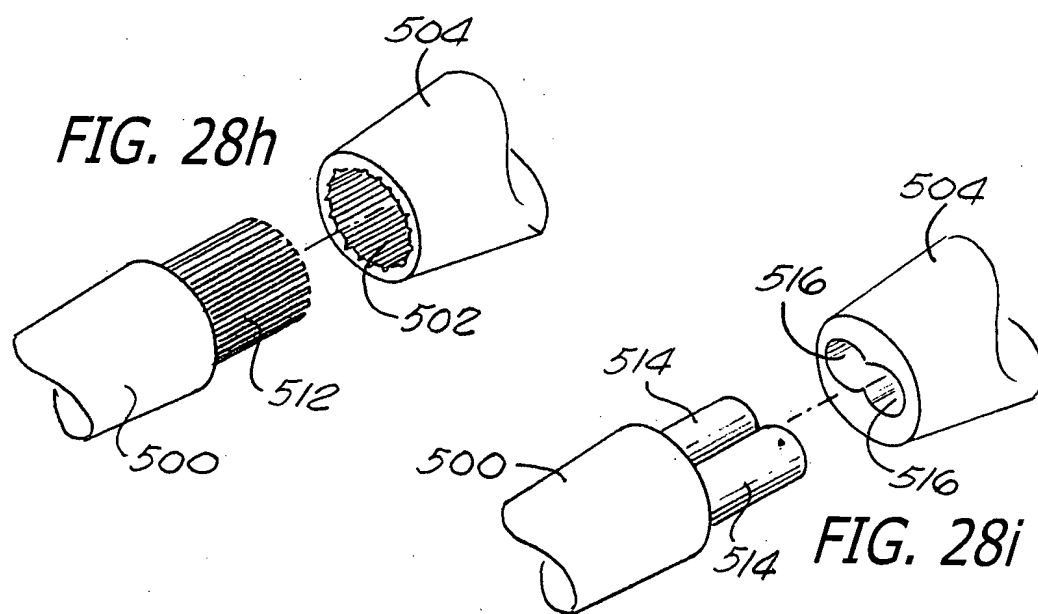
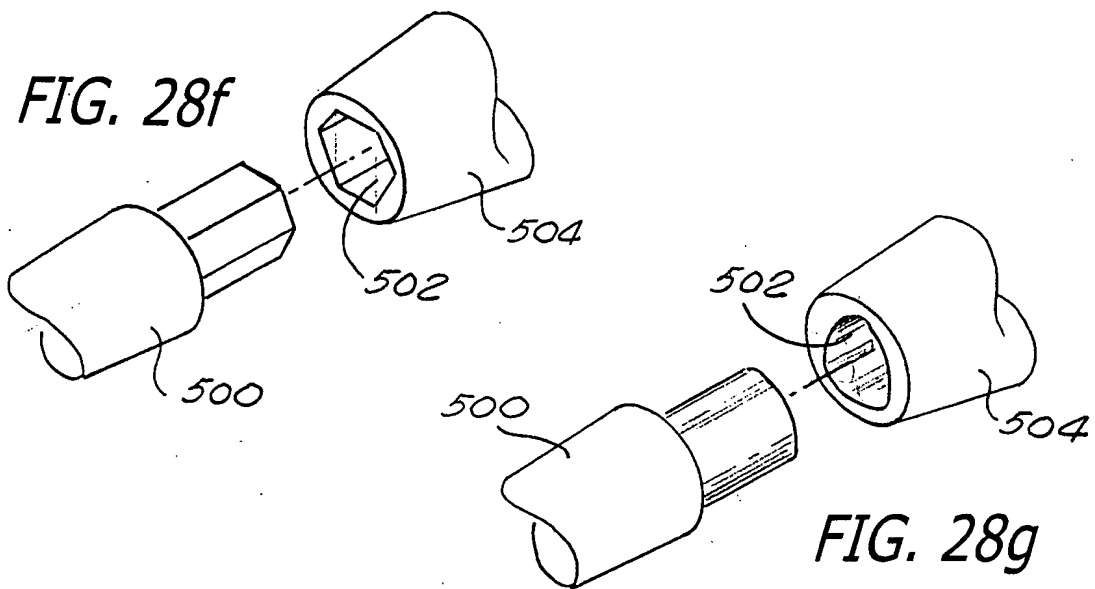


FIG. 27

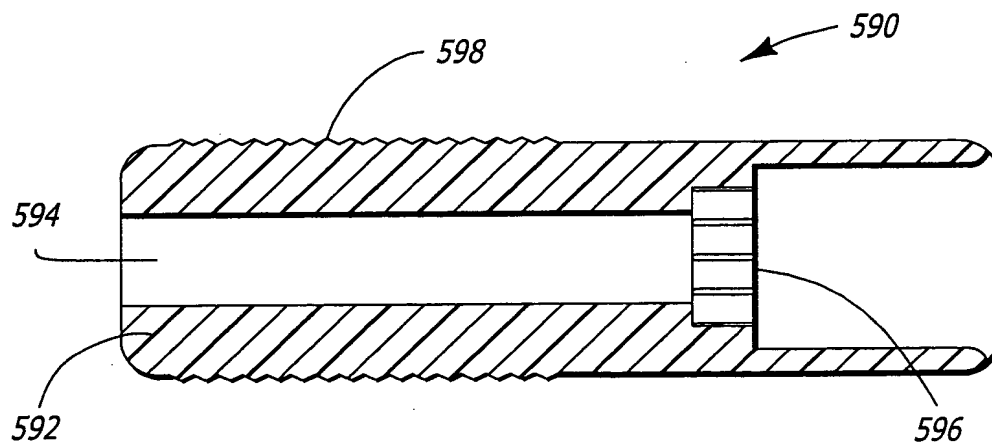
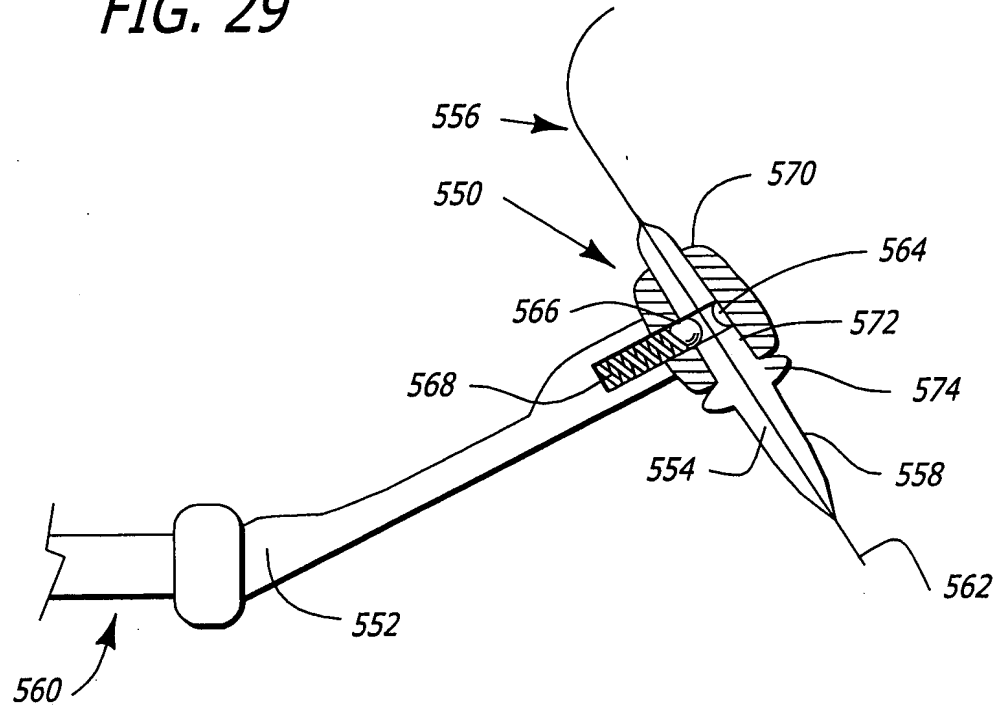




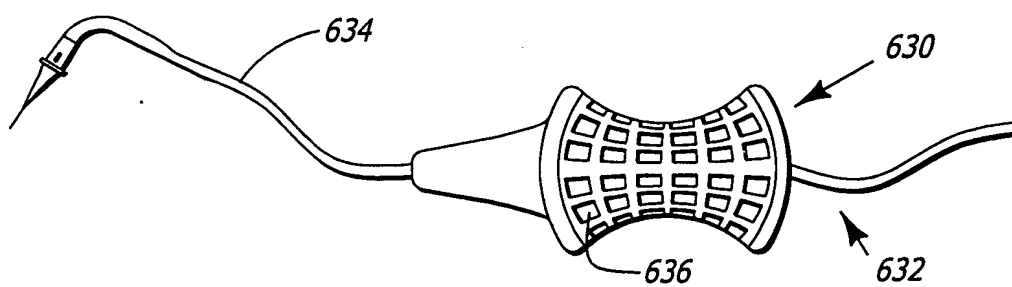
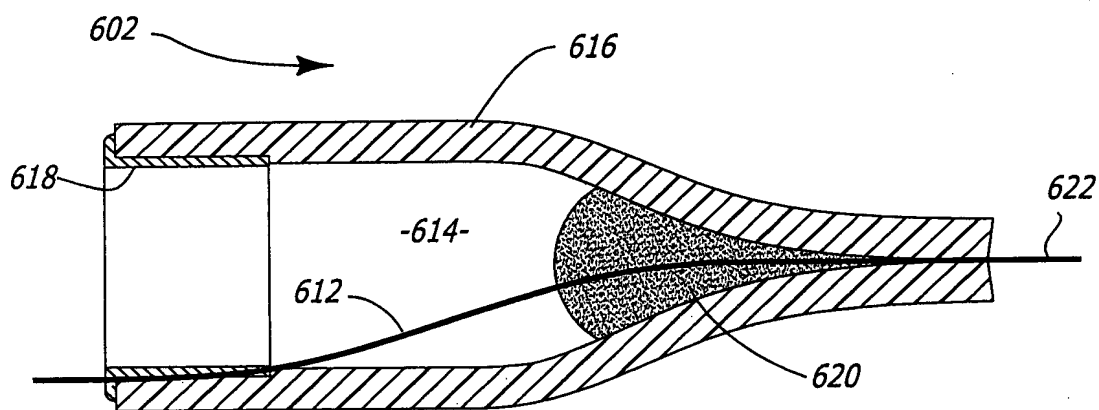
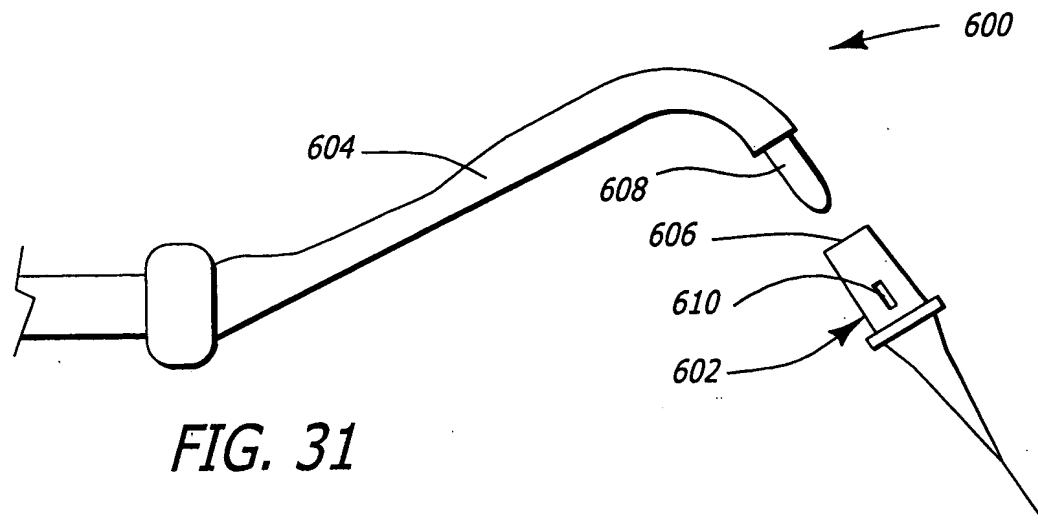


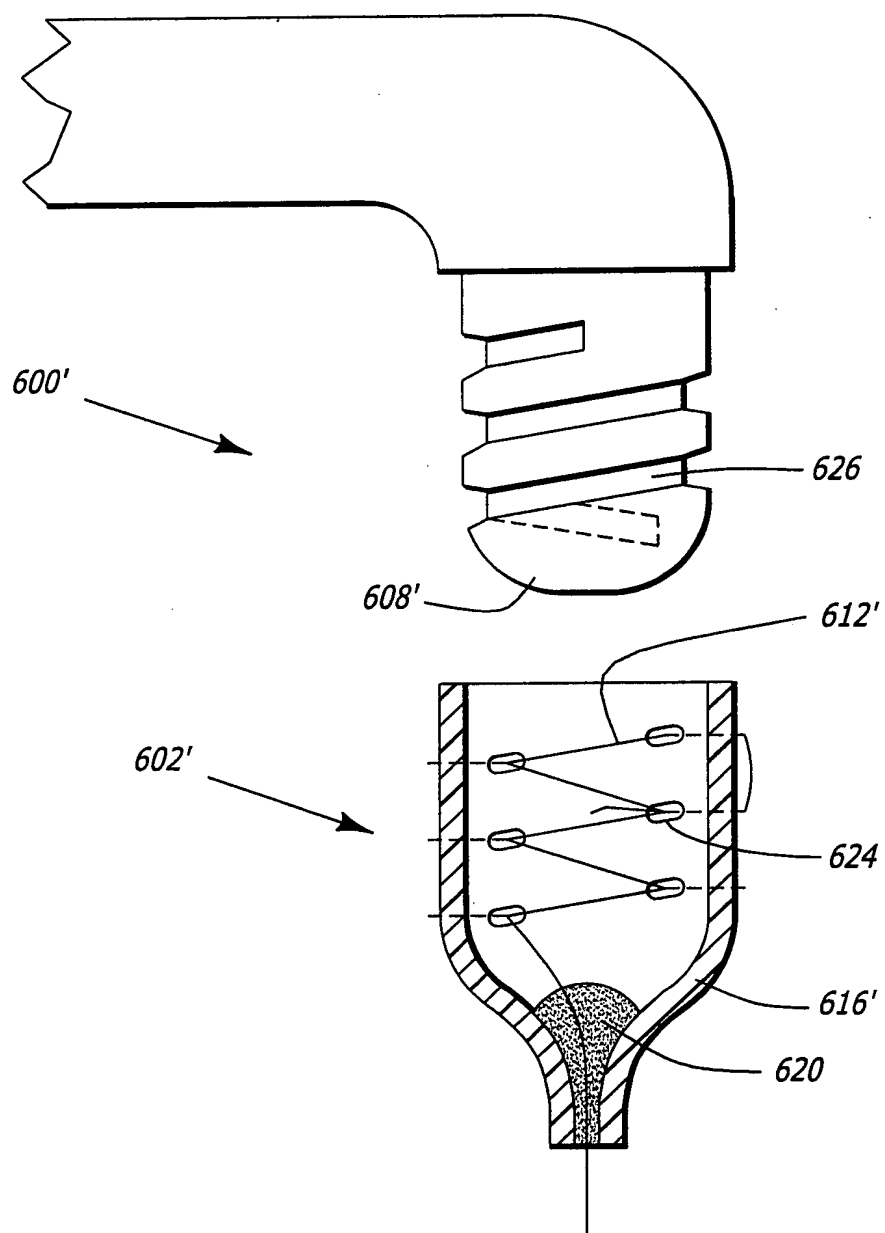


*FIG. 29*



*FIG. 30*





**FIG. 33**